**电子科技大学2023-2024学年第1学期期末考试A卷**

考试科目： 数字逻辑设计及应用 考试形式： 闭卷 考试日期： 2024 年 1 月 9 日

本试卷由 五 部分构成，共 6 页。考试时长： 120 分钟：

成绩构成比例：平时成绩 60 %，期末成绩 40 % 注：禁止使用计算器及英文辞典

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| 题号 | 一 | 二 | 三 | 四 | 五 | 六 | 七 | 八 | 合计 |
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**I. Please fill out the correct answers in the brackets “( )”.**

**( 2’×15 = 30’ )**

1. Given , then ( 0, 2, 3, 7 ),

*F* = C’ 1, 3 ) + C 0, 1 ).

2. (1110 0100)*2421BCD* = ( 1000 0100 )*8421BCD*.

3. ( 0111 0011 )*Gray*= ( 0101 1101 )2.

4. Open-drain output without pulling up has two states, Low and ( Hi-Z 或 Open 或 Floating ).

5. A *Two’s-complement*= 0110 1010, C *One’s-complement* =1111 1011, [A-C]*Two’s-complement*= ( 0110 1110 ).

Is it overflow for [A-C]*Two’s-complement*? ( No ) [Yes or No]

6. To design a “101110” serial sequence generator, ( 3 ) flip-flop(s) are needed at least. If do this design by using shift register, it should has ( 4 ) bits at least.

7. If the function , then  1, 2, 3, 6 ).

8. For an 8-bit unipolar DAC, its output voltage is 1.00V when the input is 01100100. If the input is 10001010, the corresponding output voltage will be ( 1.38 )V.

9. If a ROM has 16-bit address inputs and 8-bit data outputs, then it can be used to implement ( 8 ) combinational logic functions. Its capacity is ( 512 ) Kb.

10. A 6-bit Johnson counter without self-correcting has ( 12 ) valid states at most.

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**II. Choose the correct answer and fill in the brackets. ( 2’×10 = 20’ )**

1. Which of the following codes has the self-complementing property? ( B )

A. Gray B. 2421BCD C. 8421BCD D. Biquinary

2. Given A = (10101.11)2, its equivalent values for A10 and A16 are ( B )

A. (21.3)10, (15.C)16 B. (21.75)10, (15.C)16

C. (21.3)10, (15.3)16 D. (21.75)10, (15.3)16

3. Which of the following 2-input gates can form a complete set of logic gates? ( D )

A. XOR B. OR C. AND D. NAND

4. Which of the following gates is equivalent to XNOR? ( A )

A.  B.  C.  D. 

5. Which of the following expressions has no static hazard? ( B )

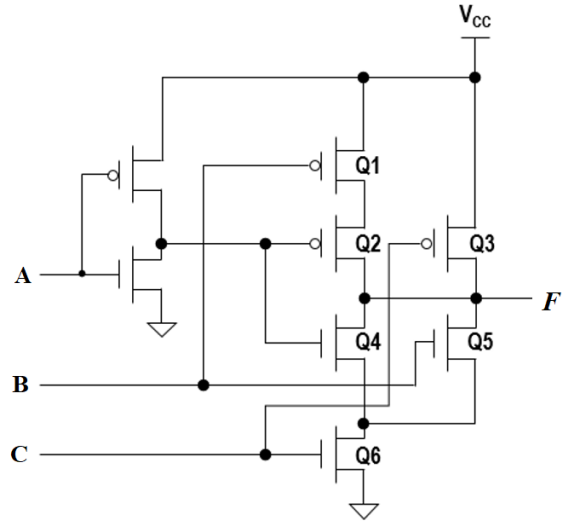
A. *F* = AC+A’D’+BC’D B. *F* = AC+A’D’+CD’

C. *F* = AC+A’D’+BC’D+CD’ D. *F* = AC+A’D’+BC’D+A’BC’

6. A CMOS circuit is shown in *Fig*. 1. The output *F* = ( A )

A. *F* = AB’ + C’ B. *F* = [(A+B’)C’]’

C. *F* = (A’+B)C D. *F* = AC’ + B’



*Fig*. 1

7. A self-dual logic function is a function such that *F* = *F*D. Which of the following functions is self-dual? ( C )

A.  B. *F* = X’YZ’+XY’Z’+X’Z

C. *F* = XY+XZ+YZ D. 

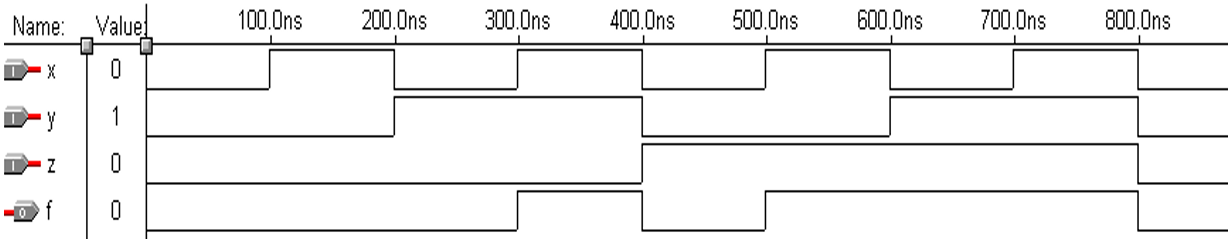
8. The minimum sum of product for AB+A’C+BCDEFGH is ( A ).

A. AB+A’C B. A’B+AC C. AB+A’C+BC D. AB+A’C+BC’

9. Given the timing diagram as shown in *Fig.* 2, the output function *f* is ( A ).

A.  B. 

C.  D. 



*Fig.* 2

10. which state is ambiguous according to the state diagram shown in *Fig*. 3? ( D )

A. A B. B C. C D. D

A

B

C

D

XY’

XY’

X’Y’

XY’

XY’

Y

Y

Y

X’Y’

X’Y’

X’Y’

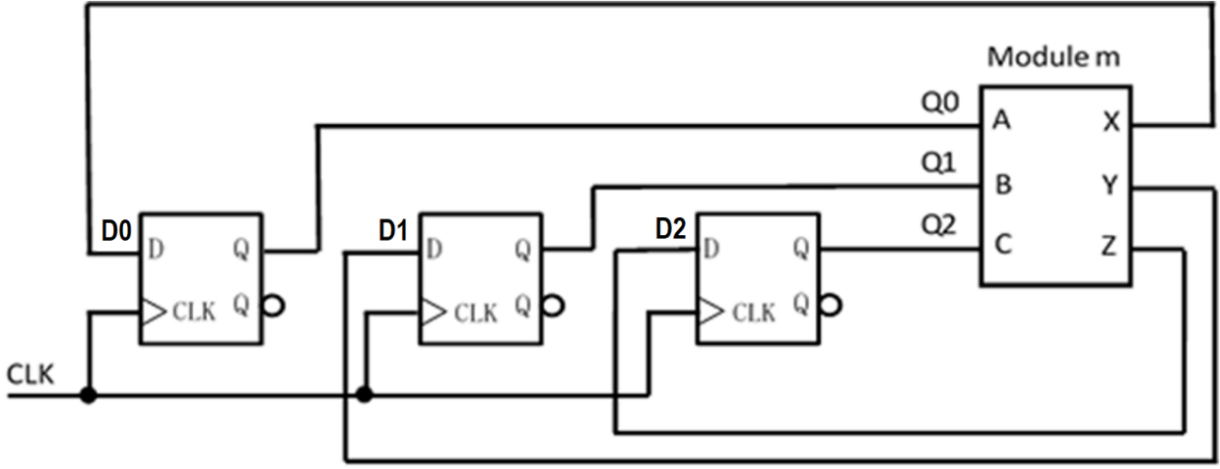
X’Y

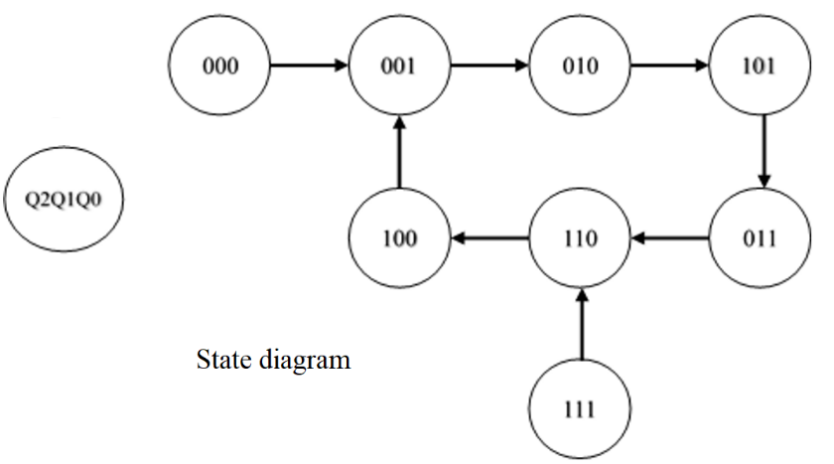
*Fig*. 3

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**III.** Sequential Logic Circuit and Verilog HDL. **(17’)**

A synchronous state machine circuit is shown below. Verilog module m is implemented to generate excitation signal for thr three D flip-flops. The function of the circuit is descripted by the state diagram shown below.

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1. Complete the transition table. [4’]

2. Write out the excitation equations. [6’]

3. Indicate the function of the circuit. [2’]

4. Please fill in the missing codes on the underlines according to your design to complete the module. [5’]

**【参考答案及评分标准】**

**1. 填写转移表，每行正确得0.5分，共4分。**

|  |  |
| --- | --- |
| Transition table | |
| Q2Q1Q0 | Q2\*Q1\*Q0\* |
| 000 | 001 |
| 001 | 010 |
| 010 | 101 |
| 011 | 110 |
| 100 | 001 |
| 101 | 011 |
| 110 | 100 |
| 111 | 110 |

**4. 每空正确得1分，共5分。**

**module m (A, B, C, X, Y, Z)**

**input A, B, C;**

**output X, Y, Z ;**

**assign Z = B ;**

**assign Y = A ;**

**assign X = ~A&~C | C&~B   
或 !A&!C | C&!B ;**

**endmodule**

**2. 激励方程每个正确得2分，共6分。**

**; ;**

**3. 自启动的模6的移位寄存器计数器。(描述正确得2分)**

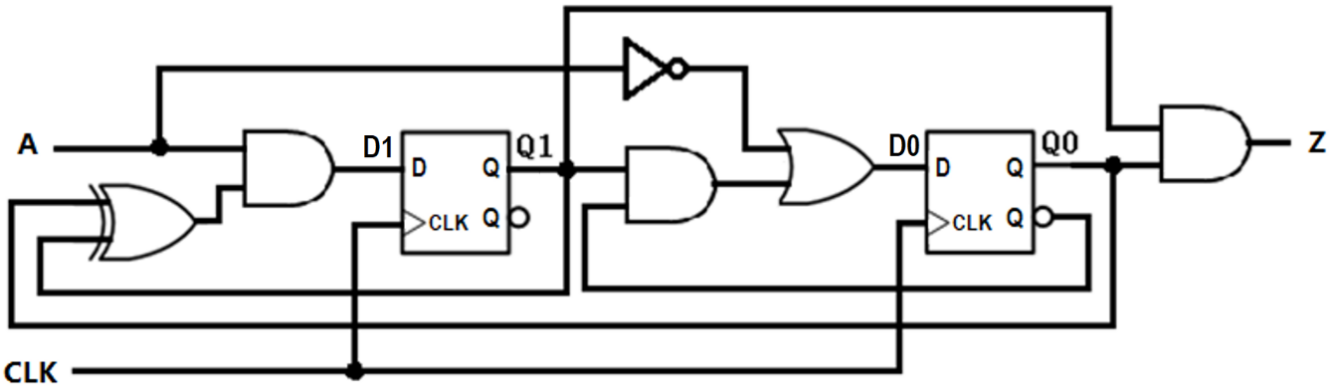
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**IV.** A synchronous state machine logic circuit is shown below. **(14’)**

1. Write out the excitation equations and output equation. [6’]

2. Complete the transition/output table. [6’]

3. Indicate the function of the circuit. [2’]



**【参考答案及评分标准】**

**1. 每个方程正确得2分，共6分。**

**2. 填写转移输出表，每空正确得0.5分，共6分。**

|  |  |  |  |
| --- | --- | --- | --- |
| Transition/output table | | | |
| Q1Q0 | A | | Z |
| 0 | 1 |
| 00 | 01 | 00 | 0 |
| 01 | 01 | 10 | 0 |
| 10 | 01 | 11 | 0 |
| 11 | 01 | 00 | 1 |
|  | Q1\*Q0\* | |  |

**3. 描述正确得2分。**

011序列检测器。

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**V.** Using a 74x163 4-bit binary counter to design a 2421BCD code counter **with the minimum cost. (19’)**

The inputs A,B,C,D of 74x163 are fixed as shown below.

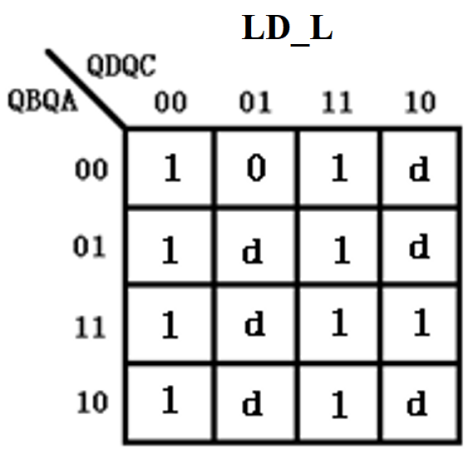
1. Using Karnaugh map, find the minimal sum-of-product expression of input LD\_L. [9’]

2. Draw a full state diagram for the counter. [8’]

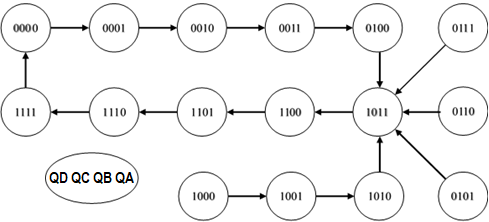
3. Complete the logic diagram [2’]

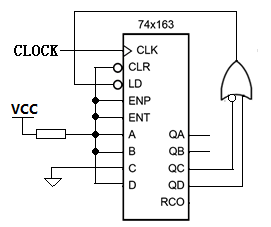
**【参考答案及评分标准】**

1. 填写卡诺图，每格正确得0.5分，最小和表达式正确得1分，共9分。



2. 画出全状态图，每个状态转移正确得0.5分，共8分。





3. 逻辑电路图正确得2分。